REMARKS

Claims 1-28 are pending in the application.

Claims 1-28 stand rejected.

Claim 1 has been amended.

Rejection of Claims under 35 U.S.C. §103

Claims 1-28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Chiussi et al., U.S. Patent No. 5,689,506 (Chiussi) in view of Somiya et al., U.S. Patent No. 6,438,107 (Somiya). Applicants respectfully traverse this rejection.

Applicants submit that Chiussi does not teach or suggest all the limitations of claim 1. Chiussi does not show, teach or suggest "combining said output queue status with said last QSP [Queue Status Parameter], forming a backpressure signal," as recited in claim 1. The non-final Office action suggests that Chiussi, in column 13, lines 39-50, teaches "combining said output queue status with said last QSP." Column 13, lines 39-50 contains a general discussion of Chiussi's technique for applying backpressure but does not show, teach or suggest combining backpressure information from one stage with backpressure information from another stage or linecard.

In response to the non-final Office action, Applicants asserted that Chiussi fails to teach the combining step of claim 1. The final Office action does not contain a direct response to Applicants' assertion; however, the following statement from the final Office action appears to suggest that Chiussi teaches the combining step: "Chiussi discloses forming a composite bitmap for all output ports and transmitting the information to each of the crossbar modules from the input stage through the fabric and onto the output

stage/output card in figure 11 (col. 13, lns. 30-50, col. 14, lns. 9-60)." The foregoing statement is unclear because Chiussi does not disclose a "composite bitmap." Furthermore, it is unclear to which of the three backpressure mechanisms of Chiussi the Office Action refers. Therefore, Applicants address how each backpressure mechanism of Chiussi fails to show, teach or suggest the combining step of claim 1.

The first backpressure mechanism disclosed by Chiussi is the mechanism for transferring backpressure information from the third stage to the second stage and from the second stage to the first stage. The third stage modules transfer third stage backpressure information to the second stage via a dedicated path, and the second stage modules transfer second stage backpressure information to the first stage via a dedicated path. (column 13, line 62 to column 14, line 24). Transferring backpressure information from one stage to another stage via a dedicated path does not suggest combining the backpressure information of multiple stages of a switch fabric; therefore, Chiussi's first backpressure mechanism could not be expected to show, teach or suggest combining a last QSP with an output queue status, as claimed in claim 1.

The second backpressure mechanism disclosed by Chiussi is the mechanism for transferring backpressure information from the first stage modules to the ingress side of the portcard. First, a backpressure bitmap is transmitted from a first stage module to the corresponding third stage module. In multiple-plane fabrics, the output stage module [third stage module] of the switch fabric multiplexes the information from each plane onto a port bitmap of outgoing modules, and the port bitmap is conveyed to the input port cards. (column 14, lines 25-54). Combining information from multiple *planes* of a single stage of a switch fabric does not suggest combining backpressure information of multiple *stages* of a switch fabric.

Thus, a "plane," as Applicants respectfully assert is understood in the art, represents a sub-unit of data at the same level in several units of data (e.g., a given bit in some number of bytes). For example, in imaging, a bit plane is a hypothetical two-dimensional plane containing a single bit of memory for each pixel in an image. In the present scenario, such a plane would be understood as a given bit, byte or other sub-unit of the datastreams being switched. In this way, a plane can be thought of as a horizontal slice of the switching architecture (e.g., the third bit of each datastream, from the switch's input, through each switching stage, to its output).

By contrast, the term "stage" embodies a given section of a system, without regard to the signals conveyed therethrough. In the context of a switching architecture, a stage can be thought of as a vertical section of the switching architecture, for example. Thus, each stage of a switching architecture switches each datastream handled by that stage. Typically, an entire datastream will be switched, although the meaning of "stage" is not changed if something less is switched. In light of the foregoing, then, Chiussi's multiplexing technique does not show, teach or suggest the combining step of claim 1.

The third backpressure mechanism implemented by Chiussi transfers backpressure information from the egress side of a port card to the third stage of the switch fabric. Each output port card transmits four bits of backpressure information to its corresponding third stage module via cells being transmitted from the ingress side of the port card to the switch fabric. (column 14, lines 55-67). Transmitting backpressure information from the egress side of a port card to the third stage of a switch fabric does not show, teach or suggest combining a last QSP with an output queue status, as claimed in claim 1. This is at least because the backpressure information of Chiussi cannot be equated with the claimed combination of last QSP and output queue status.

In conclusion, Chiussi does not disclose combining backpressure information from one stage with backpressure information from another other stage. This might be a result, at least in part, of how Chiussi uses backpressure information. Chiussi's backpressure bitmaps provide backpressure information about a stage (or port) in the switch to an upstream stage in the switch. Each stage makes enqueuing decisions based only on the backpressure information from the downstream stage. (column 13, line 30 to column 15, line 7). Because congestion is managed at each stage in the switch fabric, Chiussi would not see a need to combine backpressure (congestion) information from multiple stages of the fabric. Thus, Chiussi could not be expected to, and in fact, does not, teach combining an output queue status with a last QSP, as recited in claim 1.

Somiya does not remedy this deficiency of Chiussi. Somiya discloses a congestion bit (CI) that is set at one of the stages in the network. Somiya only discloses one congestion bit; therefore, Somiya could not disclose combining multiple congestion bits to form a backpressure signal. Furthermore, the congestion bit does not indicate the congestion status of the destination terminal (the destination terminal sets the congestion bit based on congestion information from the upstream switch). In other words, Somiya does not disclose anything comparable to an output queue status and does not teach combining congestion information from multiple stages of the network. Therefore, Somiya does not show, teach or suggest combining an output queue status with a last QSP.

Applicants submit that the foregoing arguments apply with equal force to claims 12 and 25. Applicants also submit that claims 12 and 25 are further distinguishable over Chiussi and Somiya because neither reference discloses that "said circuitry to selectively enqueue said data packet in said ingress linecard is influenced at least in part by said

backpressure signal." The backpressure signal of claims 12 and 24 includes an output queue status. Thus, the output queue status influences, at least in part, the ingress linecard enqueuing of claims 12 and 24. Neither Chiussi or Somiya shows, teaches or suggests ingress linecard enqueuing that is responsive to an output queue status.

Chiussi discloses that the backpressure information applied at the input queue is only the backpressure information from the first stage of the switch fabric. (column 9, lines 45-60 and column 13, lines 30-50). The backpressure information from Chiussi's egress queue is applied at the third stage, not at the first stage. Somiya also fails to disclose using an output queue states to perform ingress linecard enqueuing. As previously mentioned, the congestion bit disclosed in Somiya does not indicate the congestion status of the destination terminal; rather, the destination terminal sets the congestion bit based on congestion information from the upstream switch. Thus, Somiya and Chiussi both fail to disclose ingress linecard enqueuing that is responsive to an output queue status.

Furthermore, one of ordinary skill in the art would not be motivated to combine Chiussi and Somiya because a combination of the references would fail to provide any additional benefits over any such benefits already provided by Chiussi and Somiya taken separately. This is because Chiussi already has a solution to the problem recognized thereby, so provides no motivation to look elsewhere to improve that solution. Conversely, combining the teachings of Chiussi and Somiya would also fail to provide any additional advantages over Somiya taken alone because Somiya focuses on controlling cell rates and does not discuss the use of queues, as in Chiussi. Therefore, Somiya has no need to implement backpressure to keep queues from consuming too much memory, and would have no need of the techniques disclosed in Chiussi.

The Office action asserts that it would have been obvious to one of ordinary skill in the art to combine Somiya and Chiussi because this combination "would allow a centralized control instead of a distributed control as disclosed by Chiussi." Applicants respectfully submit that this conclusion is unfounded because Somiya does not disclose a centralized control system. (figure 1A and column 1, line 65 to column2, line 16).

The Office Action also suggests that adding the teachings of Somiya to Chiussi would "simplify circuitry in the switching elements [of Chiussi] since they would no longer be required to pass backpressure signals." First, Applicants respectfully submit that the resource management cells of Somiya and the backpressure signals of Chiussi cannot simply be equated with one another. Applicants respectfully submit that the resource management cells of Somiya are passed through each switch twice (as seen in figure 1A), once upstream and once downstream. If the system of Chiussi, which passes backpressure signals downstream, was modified to pass each backpressure signal both downstream and upstream, a loss would occur from more complex circuitry instead of a savings from simplified circuitry. Therefore, even if Chiussi's backpressure signals were equated with Somiya's resource management cells, one of ordinary skill in the art would not have been motivated to combine the disclosures of Chiussi and Somiya to provide Chiussi with centralized control, simplified circuitry, or to provide any additional benefits over any such benefits already provided by Chiussi and Somiya taken separately.

Applicants therefore respectfully submit that claims 1, 12 and 25 clearly distinguish over Chiussi in view of Somiya. Applicants submit that the foregoing arguments apply with equal force to claims 26-28. Applicants therefore respectfully submit that independent claims 1, 12 and 25-28, as well as claims 2-11 and 13-24, which depend on claims 1 and 12, are allowable for at least the foregoing reasons. Applicants

therefore respectfully request withdrawal of the rejections based upon 35 U.S.C §103(a). Accordingly, Applicants respectfully submit that claims 1-28 are in condition for allowance.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5084.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 15, 2005.

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